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Feature Article

Pentacene devices: Molecular structure, charge transport and photo response

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In this feature article, we will discuss to which extend the peculiar growth properties of pentacene on metallic contacts and on gate dielectrics contribute to the device performance of organic thin film transistors. The early growth state of pentacene monolayers is reviewed, as well as the molecular structure of the so called thin film phase. Then, the relation of structural defect densities to trap densities is discussed. The spatially resolved photo response of a pentacene transistor will be presented in the context of injection barriers and contact homogeneity.

1 Introduction Today, the field of organic electronics is wide open [1, 2]. While organic light emitting diodes (OLEDs) have already successfully entered the market, the roadmap for integrated circuits is still not settled. Mobilities μ for pentacene organic thin film transistors (OTFTs) commonly ranging between 0.1 cm/V s and 1 cm/V s have been reproduced by many groups world wide [3–6]. In spite of the enormous activities in synthesizing and screening for new materials for transistor applications, pentacene has successfully defended its leading position for the production of OTFTs.

The reason for pentacene being superior for the production of TFT devices [7, 8] when compared to other molecules [9] is still not obvious. In this feature article, we will discuss to which extend the peculiar growth properties [10] of pentacene on metallic contacts and gate dielectrics contribute to the device performance. For this purpose, first the early growth state of pentacene films and the molecular structure of the so called thin film phase is reviewed. Then, major sources of crystal defects in thin films as determined by advanced synchrotron diffraction techniques are discussed. The relation of these defects to the frequently discussed electronic traps that strongly influence transport properties of TFTs [6, 11, 12] is indicated.

Finally, the spatially resolved photo response of pentacene OTFTs will be discussed in the context of injection barriers and contact homogeneity.

2 Pentacene thin films

2.1 Film formation on inert surfaces Pentacene can be evaporated quite conveniently by resistive heating of a tantalum crucible filled with purified pentacene powder. This procedure is ultra high vacuum compatible and a molecular beam with typical deposition rates ranging from below 0.01 nm/s up to 1 nm/s can be easily achieved [13], as verified by a quartz micro balance at the sample position. Also alternative methods such as laser evaporation have been reported [14]. Growth temperatures typically range from room temperature up to 50 °C. At higher temperatures, a much higher deposition rate is needed to compensate for desorption. Thus, with MBE techniques, the maximum growth temperature is limited to about 75 °C. A typical example for a pentacene film grown on a thermal oxide with Au bottom contacts is shown in Fig. 1a. If substrate and growth conditions are properly chosen, a continuous film forms on SiO_2 (Fig. 1a) with grains of the order of several microns which exhibit step heights comparable to the length of the pentacene molecule (Fig. 1b). On

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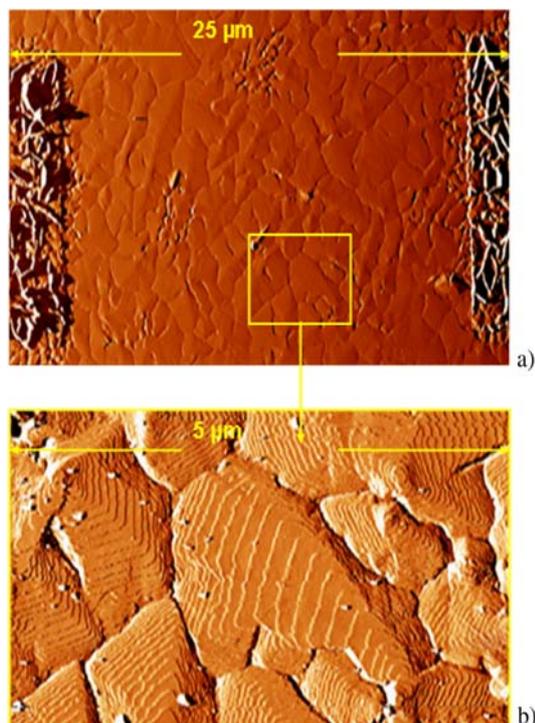
Figure 1 (online colour at: www.pss-a.com) AFM amplitude micrograph of a pentacene OTFT structure. (a) Gold contacts on SiO$_2$ have been covered by a 50 nm pentacene film. (b) A zoom reveals a grainy structure and terraces with step heights of ca. 15.4 Å.

the gold contacts, the film morphology is much more rugged (Fig. 1a). The reason for the profound difference in growth behavior on SiO$_2$ and Au is discussed below.

The initial stage of pentacene thin film growth on SiO$_2$ can be described by diffusion limited aggregation (DLA) [15]. In this growth mode, incoming molecules initially diffuse across the surface. Once they meet a critical number of molecules, they form a stable nuclei, which subsequently grows in area during deposition. The submonolayer islands stemming from the growth of such nuclei exhibit a fractal shape, which is the fingerprint of this growth mode. Pentacene submonolayers grown on bare Si surfaces show such fractal shapes, as revealed first by in-situ photo electron emission microscopy experiments [16]. Subsequent AFM studies have shown that the diffusion length on silicon oxide is significantly reduced [17] compared to e.g. H-terminated Si. A detailed analysis of the island size and island density as a function of coverage by AFM and synchrotron experiments fully confirmed scaling predictions of the DLA theory [18, 19] and allowed to determine the stable nuclei size to four pentacene molecules [20]. If the growth temperature is lowered to 0 °C, the diffusion length is reduced by a factor ~4 [20].

Pentacene submonolayer islands exhibit a layer thickness of 15.4 Å which has been measured by AFM and by X-ray reflectometry [17]. This layer thickness implies that the molecules are oriented in an upright configuration, i.e.
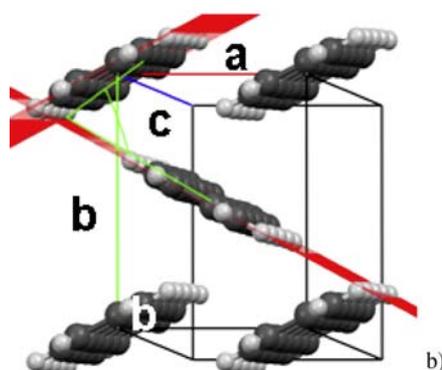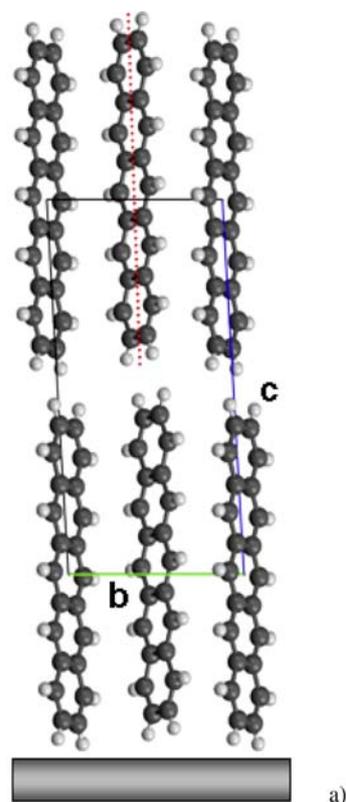
Figure 2 (online colour at: www.pss-a.com) Thin film phase unit cell. (a) The side view illustrates the layered structure of the thin film phase. (b) The top view emphasizes the herringbone ordering motive, which is a common feature of all pentacene polymorphs.

the long molecular axis is oriented predominantly along the surface normal, see Fig. 2a. Multilayer films exhibit different crystalline phases, which are usually identified by their d_{001} spacing along the surface normal. The substrate-induced $d_{001} = 15.4$ Å polymorph, which is commonly termed *thin film phase*, is the most relevant for OTFT applications. Grazing incidence in plane diffraction experiments [21, 22] confirmed that the grains of the thin film phase are (001) oriented. The lateral dimension of the two dimensional unit cell inferred from these experiments, as well as the observed selection rules, suggest a unit cell

with two non-equivalent molecules in a Herringbone arrangement, similar to the bulk pentacene ordering motive [23, 24].

In a recent study, the detailed molecular arrangement of the *thin film phase* was resolved by a grazing incidence truncation rod scattering study [25]. The crystal structure was found to be triclinic [26] with the following unit cell parameters: $a = 5.958 \pm 0.005$ Å, $b = 7.596 \pm 0.008$ Å, $c = 15.61 \pm 0.01$ Å, $\alpha = 81.25 \pm 0.04°$, $\beta = 86.56 \pm 0.04°$ and $\gamma = 89.80 \pm 0.10°$ [27]. A detailed analysis of the Bragg peak intensities for pentacene on SiO_2 allowed to determine the tilt between the long molecular axis of the two unit cell molecules and the surface normal to $5.6 \pm 0.05°$ and $6.0 \pm 0.4°$ and the Herringbone angle to $54.3 \pm 1.3°$ [27]. The unit cell is shown in Fig. 2b). Here, the unit cell vectors *a* (red), *b* (green) and *c* (blue) are color coded. The Herringbone angle (green arc) is defined as the intersection angle between molecular planes (red planes). In one case, also a molecular axis (red dotted line) is indicated.

Surface energy calculations [28] reveal that the (001) cleaving plane is the surface with the lowest surface energy. In turn, the formation of (001) oriented films can be expected, if the interaction of the pentacene molecules with the surface is negligible to the pentacene–pentacene interaction. Experiments show that this condition apparently fulfilled for various inert substrates such as reduced and oxidized Si, as well as many polymeric films used as gate dielectric. Note that the surface energy of the *thin film phase* is rather isotropic within the pentacene film plane [28], probably a direct result of the large herringbone angle. In turn, pentacene islands show on SiO_2 a rather isotropic shape, thus favoring the formation of closed films up to several monolayers [16, 29]. Beyond this thickness, strong roughening occurs [30] and competing phases start nucleating [31].

2.2 Film formation on metallic and conductive surfaces
Bottom contact TFTs involve either metallic or conducting polymer contacts. Therefore, the growth of pentacene on metallic surfaces has also been studied in detail [32–35]. The most commonly used contact material for pentacene TFTs is Au, whose work function value $\phi = 5.1$ eV [36] matches quite well with the ionization energy of pentacene $\chi = 4.9$ eV [37]. Also, being a noble metal, Au contacts are sometimes considered insensitive to air exposure even if it has been observed that the Au work function is quite sensitive to ambient conditions. The observed growth behavior for pentacene on Au depends strongly on the substrate, i.e. different growth is observed for single Au crystal surfaces [32] and for thin Au film composed out of polycrystalline grains [33]. Also the roughness and cleaning procedure influence the growth. For the technically most relevant polycrystalline Au film surfaces, pentacene shows a complex growth behavior. If a Au(111) texture is present, a flat lying monolayer forms, which can be interpreted as a wetting layer. This layer then
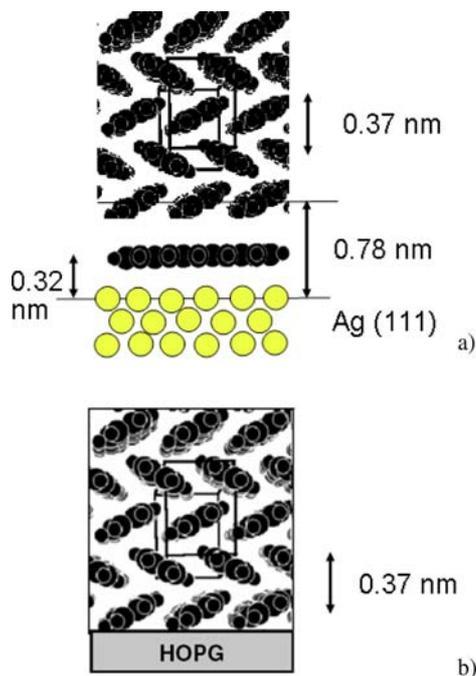
Figure 3 (online colour at: www.pss-a.com) Pentacene growth on Ag and graphite. (a) Side view of the film structure of pentacene on Ag(111). A flat lying pentacene monolayer acts as a growth template. (b) Side view of the growth of pentacene on graphite. The structure resembles the growth on Ag, but it is not clear whether a pentacene wetting layer is present.

acts as a growth template for subsequently deposited pentacene forming microscopic grains. For these grains, the long molecular axis is oriented along the surface (*lying down phase*). Elevated temperatures promote a pronounced dewetting [34]. This behavior is not unexpected, since the surface energy of a *lying down phase* is higher than the surface energy of the *thin film phase* [28] and thus dewetting is a direct result of the minimization of the film surface area. Thus, surface diffusion is counter-productive for the formation of closed films and the formation of well ordered closed films seems quite impossible. To resolve this problem, two strategies have been pursued. One approach, which has been demonstrated for single crystal Ag(111) surfaces makes use of cryogenic substrate temperatures to suppress dewetting. In this case, the pentacene molecules are deposited making use of a hyperthermal He-beam [38] which provides the impinging pentacene molecules with energies up to 5 eV, well above thermal energies. Thus, a well ordered film can form at 200 K [35] (see Fig. 3a).

Another way to avoid dewetting is to passivate the metallic surface by a self assembled monolayer (SAM), e.g. an alkane thiol monolayer (C-18). After passivation, the growth structure resembles the growth mode on inert surfaces [33], the same holds for growth of pentacene on conducting polymers such as PEDOT: PSS [poly(3,4-ethylenedioxythiophene)/poly(styrenesulfonate)] [39]. It is interesting to note that on bare Si, pentacene initially forms a flat lying monolayer, but on-top of this monolayer, the

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thin film phase readily forms [16] without need for passivation.

Other more exotic materials which have been studied include graphite and Bi. Graphite is an interesting substrate since it also promotes the formation of a *lying down phase* with Herringbone order textured in the (200) orientation [40] (see Fig. 3b). This enabled an angular resolved photoelectron emission study (APES) for this pentacene polymorph along the (200) direction of the Brillouin zone. The experiments reveal indications of strong band dispersion [40]. Recently, a well defined epitaxial relationship between a pentacene film and the Bi substrate has been realized. This well defined epitaxial relationship allowed to explore the band dispersion of different crystallographic directions of the Brillouin zone of pentacene by APES, also revealing a pronounced band dispersion [41].

2.3 Mixed films For some applications such as organic photovoltaic devices or ambipolar transistors, a co-deposition of hole and electron conducting materials is needed, e.g. pentacene and C60. This gives rise to a whole zoo of possible growth scenarios, depending on how the different materials mix. For the co-deposition of pentacene and 6,13-pentacenequinone (an oxidized state of pentacene) a pronounced phase separation is observed, depending on deposition rates [42]. At the same time, the formation of the pentacene bulk phase is suppressed in mixed film.

3 Pentacene OTFT properties

3.1 Mobility and charge carrier density The most simple pentacene OTFT test structure used in many labs is based on a Si wafer piece covered with a thermal oxide. Here, the heavily doped Si wafer takes the role of the back gate electrode, and the SiO_2 takes the role of the gate dielectric. A pentacene thin film is deposited as the semiconducting layer. Source and drain electrodes are deposited either on the silicon oxide (bottom contact) or on top of the pentacene film (top contact).

A pentacene TFT works in hole accumulation, i.e. a sufficiently negative voltage (V_G) is applied to the gate, accumulating holes at the pentacene/SiO_2 interface. If now a moderate voltage is applied between the source and drain electrode, a hole current flows. A characteristic output curve for a typical pentacene TFT from our lab is shown in Fig. 4a. Here, as a substrate, heavily n-doped Si-wafers with a 150 nm thick thermal SiO_2 layer on top of it were used. Additionally, a very thin layer of polysterene (ca. 2−3 nm) was spin cast on top of the silicon oxide layer. A shadow mask was used to define 50 nm thick source and drain Au contacts that were evaporated in vacuum. Finally a 50 nm pentacene layer was evaporated at room temperature at a deposition rate of about 1 nm/min in a separate evaporation chamber, also using a shadow mask. This way, transistor channels with a length of $L = 25\,\mu m$ and a width of $W = 1000\,\mu m$ were obtained, cf. schematic in Fig. 4. The output curve of this device shows a linear increase of the
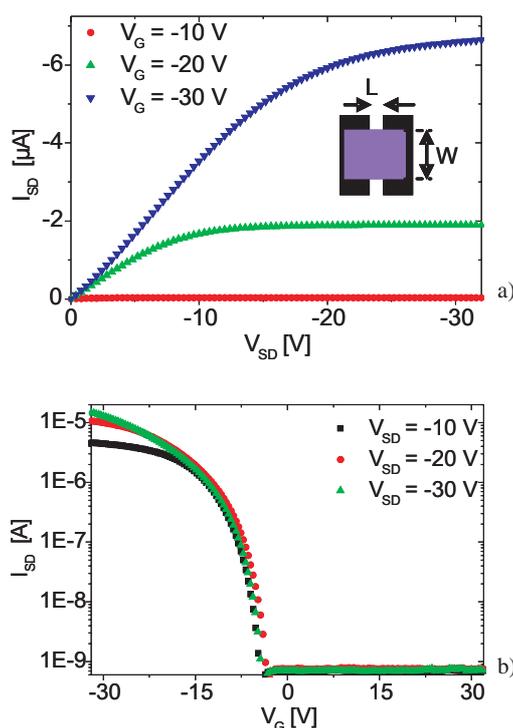
Figure 4 (online colour at: www.pss-a.com) Characteristics of a bottom contact pentacene OTFT. Channel geometry: $L = 25\,\mu m$, $W = 1000\,\mu m$ (see text and inset). Sweep rate: 0.4 V/s, the measurement was performed in vacuum. (a) Output characteristics (I_{SD} vs. V_{SD}, V_G as indicated in the inset) and (b) transfer characteristics (I_{SD} vs. V_G in log. scale, V_{SD} as indicated in the inset).

drain current for small drain voltages, and subsequently saturation occurs. The transfer characteristics of this device are shown in Fig. 4b. The logarithmic scale reveals a sharp onset of the transistor activity and a subthreshold swing $S = V_G/\log(I_{SD}) = 1.1$ V per decade.

Pentacene OTFT curves are usually analyzed within MOSFET theory [43]. For the geometry of the device used in Fig. 4, which has a channel width $W = 1000\,\mu m$ and a channel length $L = 25\,\mu m$, the source-drain current (I_{SD}) in the linear regime ($V_{SD} \ll V_G - V_T$) can be written as:

$$I_{SD}^{lin} = W/L \cdot \mu^{lin} \cdot C_i \cdot (V_G - V_T) \cdot V_{SD}\,. \tag{1}$$

Here, the graded channel approximation has been used. C_i is the capacitance per unit area of the dielectric and V_T is the threshold voltage. μ^{lin} is the mobility in the linear regime. The respective measurements are shown in Fig. 5a.

For the saturation regime ($V_{SD} \gg V_G - V_T$) the accumulation within the channel is incomplete. This so called *pinch off* arises due to the superposition of the gate and drain potential. The source−drain current (I_{SD}) in the saturation regime reads:

$$I_{SD}^{sat} = W/(2L) \cdot \mu^{sat} \cdot C_i \cdot (V_G - V_T)^2\,. \tag{2}$$

The respective measurements are shown in Fig. 5b. The mobility in the saturated regime (μ^{sat}) can be read off from the slope of the output curve (straight lines in Fig. 5b,
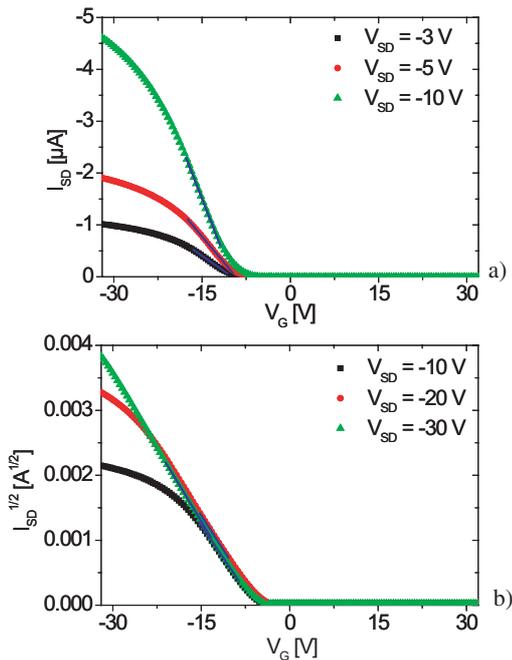
Figure 5 (online colour at: www.pss-a.com) Transfer characteristics. (a) Linear regime (I_{SD} vs. V_G), the straight lines indicate the slope determining μ^{lin} according to Eq. (1). (b) Saturated regime ($\sqrt{I_{SD}}$ vs. V_G), the straight lines indicate the slope determining μ^{sat} according to Eq. (2). Same device as in Fig. 4.
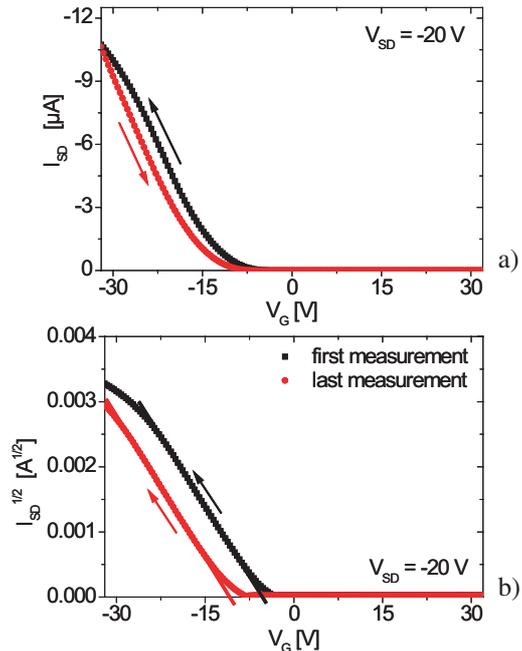

Figure 6 (online colour at: www.pss-a.com) Hysteresis effects and voltage drifts in the transfer characteristics. Sweep rate is 0.4 V/s, same device as in Fig. 4. (a) A gate sweep from positive to negative voltages (black data points), and back (red data points) for the same fixed value of the drain voltage ($V_{SD} = -20$ V) reveals a hysteresis effect. (b) After a couple of measurements (one hour later), a rather stable shift of the transfer curve due to fixed charges is established for the same device.

square root scale at y-axis) using Eq. (2). We obtain $\mu^{sat} = 0.06$ cm^2/(V s), which compares reasonably well to typical values for the bottom contact geometry ($\mu \approx 0.1 - 0.3$ cm^2/(V s)). The mobility in the linear regime (μ^{lin}) can be read off from the slope of the output curve (Fig. 5a, linear scale at y-axis) using Eq. (1). We obtain $\mu^{lin} = 0.04$ cm^2/(V s), which is slightly reduced compared to $\mu^{sat} = 0.06$ cm^2/(V s), indicating some non-ideal behavior.

The most important physical parameter of an OTFT beyond the mobility μ is the number of charge carriers (n_h) induced by a given gate voltage (V_G). n_h can be estimated from the measured channel conductivity σ by

$$n_h \cdot q \cdot \mu = \sigma/d = L/(W \cdot R). \tag{3}$$

Here, d is the active channel thickness ($1-2$ molecular layers) and q is the elementary charge of a hole. For the transistor used in Fig. 4, we measure $R = 2.8 \times 10^6$ Ω at $V_G = -30$ V and $V_{SD} = -10$ V. In turn, according to Eq. (3), the hole carrier density at this set point is $n_h = 0.9 \times 10^{12}$ cm^{-2}.

3.2 Influence of trap states and fixed interface charges An example for the dynamic behavior of a pentacene OTFT is shown in Fig. 6a. Here, the gate voltage (V_G) is first swept from positive to negative voltages (sweep rate

= 0.4 V/s, black data points in Fig. 6a), and then immediately from negative to positive voltages (red data points in Fig. 6a) for the same fixed value of the drain voltage ($V_{SD} = -20$ V). A pronounced hysteresis is observed. This hysteresis can be interpreted as an apparent shift of the threshold voltage (ΔV_T) induced by a charging Q_t of the pentacene/SiO$_2$ interface due to filling and emptying of trap states. The number of trap states can be estimated by

$$n_t = Q_t/q = \Delta V \cdot C_i/q. \tag{4}$$

The observed threshold shift of $\Delta V_T = 2.0$ V results in a trap density $n_t = 2.4 \times 10^{11}$ traps/cm^2. This number is not so small compared to the number of charge carriers n_h, indicating that traps largely influence the device performance. One may speculate whether structural defects within the pentacene film contribute to trap states. An X-ray analysis of the defect densities in pentacene films revealed defect densities in the order of $n_t = 2 \times 10^{11}$ defects/cm^2 [44], in good agreement with the trap density n_t inferred from the electronic characterization. Thus, the observed structural defects apparently contribute to trap states. It is well known, that the hysteresis and thus the trap density depends on the nature of the gate dielectric surface. Especially hydroxyl groups are considered as potential trap

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states, therefore a passivation of the gate oxide by either si-lanization [45] or polymer capping (here: polystyrene film) is needed to minimize trap densities.

A subsequent study of the pentacene TFT reveals also an irreversible drift of the transfer curve with operating time, cf. Fig. 6b. This drift can be interpreted as an inter-face charging due to deep trap levels, also termed fixed charges. The observed voltage shift of $\Delta V = 6.5$ V implies a fixed charge density $n_{dt} = 7.7 \times 10^{11}$ cm^{-2}. Note that this density is already of the order of the charge carrier density n_h. In turn, voltage shifts in pentacene TFTs can com-pletely redefine the working point of a transistor. For the application of such TFT devices in e.g. ring oscillators [46], one should find a way to control these drifts. Recent work suggests that controlled generation of fixed charges at the gate dielectric by UH-light exposure might be used to store electronically readable information in a pentacene TFT (one bit per transistor).

3.3 Injection The whole TFT performance is largely influenced by injection efficiencies. In particular surface contaminations such as remanent photo resist or organic adsorbates due to air or solvent exposure can modify the work function of the Au electrode up to a point, that charge injection is locally suppressed. The injection properties of two selected TFT devices from our lab are compared in Fig. 7. Both devices are operated at $V_G = -30$ V. The out-put characteristics of the two devices show a pronounced difference for small drain voltage V_{SD}. While one device (so called *good device*, black data points in Fig. 7) shows an ohmic increase of I_{SD} as a function of V_{SD}, the other de-vice shows a damped response (so called *bad device*, red data points in Fig. 7). Note that the amplitude of I_{SD} of the bad device has been rescaled for better comparison. Both devices are bottom contact TFTs of similar geometry, however, the preparation of the contacts was different. The contacts of the good device were fabricated using a shadow mask, while the contacts of the bad device were produced using optical lithography. Optical lithography involves
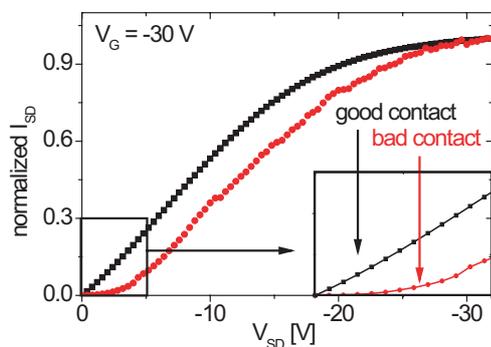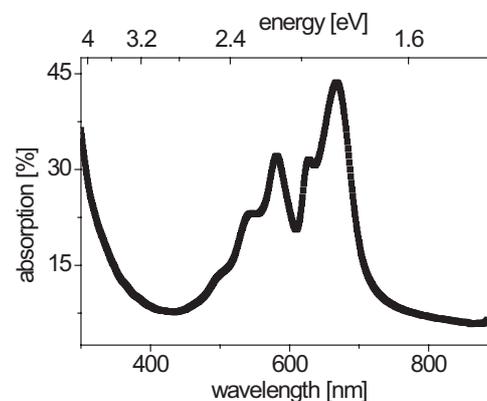
resist and use of solvents such as acetone, which appar-ently can lead to less efficient contact properties. The physical mechanism which gives rise to the non-ohmic be-havior remains unclear at this level of analysis and thus us-ing equivalent circuits [47] which take account of the ob-served deviations from ideal MOSFET behavior seem to be the most practical way to deal with these effects.

4 Photoresponse Pentacene shows a strong absorp-tion in the visible (see Fig. 8), more optical properties of pentacene films can be found in [48]. If pentacene is com-bined with a proper n-conductor such as C60, it can be used as active region in a solar cell [49]. Transient photo-conductivity experiments using optical pump terahertz probe techniques suggest that charge photo generation oc-curs in pentacene on a subpicosecond timescale [50].

Here, we employ photo generated electron–hole pairs to analyze local properties of a TFT device. For this pur-pose, we have adapted a laser scanning confocal micro-scope experiment to spatially resolve the photo response of a TFT. The experimental setup is shown schematically in Fig. 9a. The laser spot size on the TFT is less than 1 µm. A $x–y–z$ piezo-positioner stage [51] which is mounted on top of a $x–y$ translation stage is used to translate the sample with respect to the laser. The reflected beam allows to identify the contact and the channel region. The laser beam is modulated by a chopper, and the difference signal is ex-tracted using a lock-in amplifier.

We observe a strong photo response localized at the anode [52]. The response is inhomogenous along the con-tact indicating variations in the transport or injection prop-erties of the device. These variations may be due to local variations of the contact work function, or due to bad physical contact of the pentacene grains adjacent to the electrode, or due to a local enhancement of defect densities in the pentacene film. Thus, a systematic study of the photo response in combination with the respective charac-teristic transistor curves allows visualizing problematic re-gions of an OTFT, which is a key prerequisite for device optimization.

Figure 7 (online colour at: www.pss-a.com) Injection efficien-cies of pentacene TFTs. Comparison of ohmic and non-ohmic behavior. The contacts of the so called *good device* were fabri-cated using shadow masks, and the contacts of the so called *bad device* were fabricated using optical lithography.

Figure 8 Absorption spectra. Wavelength dependency of the ab-sorption of a 50 nm pentacene thin film on glass.
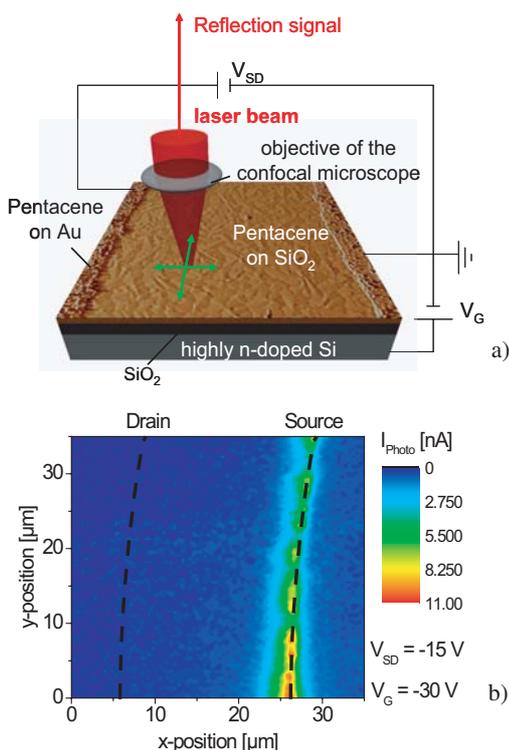
Figure 9 (online colour at: www.pss-a.com) Spatially resolved photo response experiment. (a) Schematic of the experimental setup for spatially resolved photo response measurements. (b) Spatially resolved photo response data in the linear regime ($V_G = -30$ V and $V_{SD} = -15$ V). A Corbino device structure has been used (disk and ring geometry, $L = 20\,\mu m$ [channel length], $W = 1005\,\mu m$ [channel width, i.e. circumference]). The photo response measurement covers a small fraction of the whole device.

5 Outlook Pentacene has all the qualities needed for an OTFT. The main challenge is the control of the contact and dielectric interfaces to suppress the voltage drifts and hysteresis effects associated with trap states. Also the dependency of the injection efficiencies on contact preparation suggest that even if pentacene deposition technology can be applied under rather rough conditions, ultra high vacuum and clean environments may still be useful on the way of learning how to produce reliable devices.

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